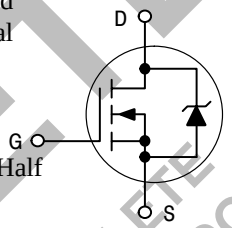
Designer's™ Data Sheet

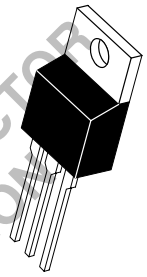
TMOS E-FET ™
Power Field Effect Transistor
N−Channel Enhancement−Mode Silicon Gate

MTP12N10E

Motorola Preferred Device

TMOS POWER FET
12 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.16 OHM





CASE 221A−06, Style 5
TO−220AB

This advanced TMOS E−FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain−to−source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Designed to Eliminate the Need for External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source−to−Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	100	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate−Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	12 30	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	79 0.53	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C

UNCLAMPED DRAIN−TO−SOURCE AVALANCHE CHARACTERISTICS ($T_J \le 175$°C)

Single Pulse Drain−to−Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, L = 4.03 mH, R_G = 25 Ω, Peak I_L = 12 A) (See Figures 15, 16 and 17)	E_{AS}	290	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.9 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (positive)			—	110	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 V, V_{GS} = 0)		I_{DSS}	—	—	10	μA
(V_{DS} = 100 V, V_{GS} = 0, T_J = 150°C)			—	—	100	
Gate−Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate−Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (negative)			—	6.0	—	mV/°C
Static Drain−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.125	0.16	Ohm
Drain−Source On−Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 12 Adc)			—	1.5	2.4	
(I_D = 6.0 Adc, T_J = 150°C)			—	1.4	1.92	
Forward Transconductance ($V_{DS} \geq$ 15 V, I_D = 6.0 A)		g_{FS}	4.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 14	C_{iss}	—	600	—	pF
Reverse Transfer Capacitance		C_{rss}	—	70	—	
Output Capacitance		C_{oss}	—	230	—	
SWITCHING CHARACTERISTICS (T_J = 100°C)						
Turn−On Delay Time	(V_{DD} = 50 V, I_D = 12 A, V_{GS} = 10 V, R_G = 12 Ω) See Figure 7	$t_{d(on)}$	—	10	—	ns
Rise Time		t_r	—	64	—	
Turn−Off Delay Time		$t_{d(off)}$	—	21	—	
Fall Time		t_f	—	30	—	
Gate Charge	(V_{DS} = 80 V, I_D = 12 A, V_{GS} = 10 Vdc) See Figures 5 and 6	Q_T	—	18	26	nC
		Q_1	—	4.0	—	
		Q_2	—	10	—	
		Q_3	—	8.0	—	
SOURCE−DRAIN DIODE CHARACTERISTICS*						
Forward On−Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	—	1.0	2.5	Vdc
	(I_S = 12 A, V_{GS} = 0, T_J = 150°C)		—	0.83	—	
Reverse Recovery Time	(I_S = 12 A, V_{GS} = 0, dI_S/dt = 100 A/μs, V_R = 50 V)	t_{rr}	—	110	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

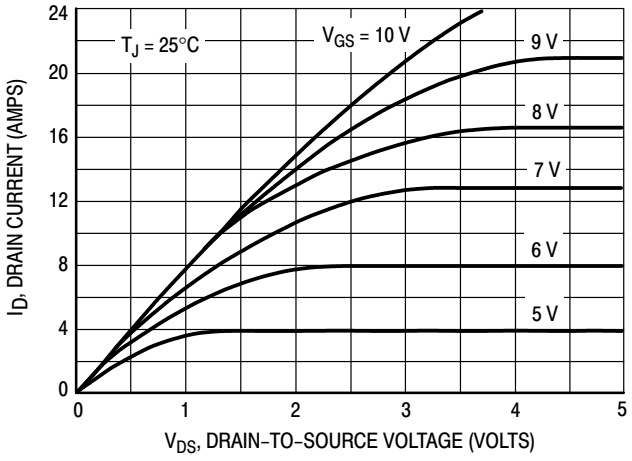


Figure 1. On−Region Characteristics

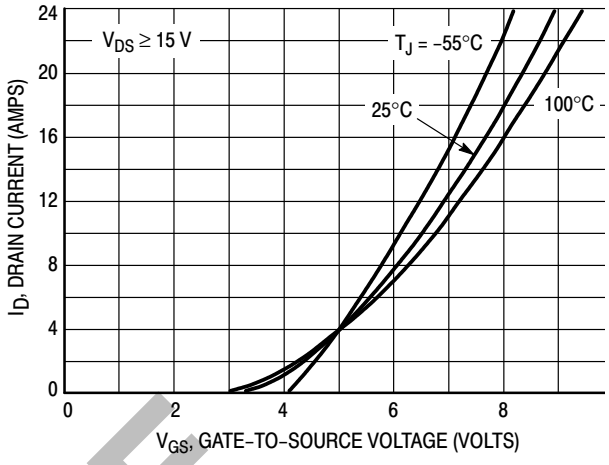


Figure 2. Transfer Characteristics

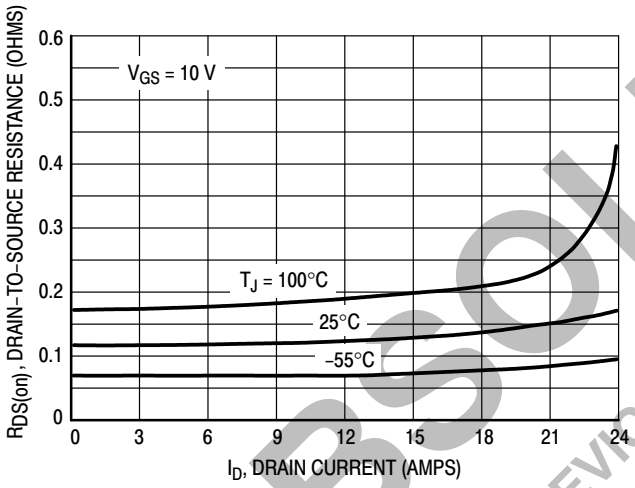


Figure 3. On−Resistance versus Drain Current

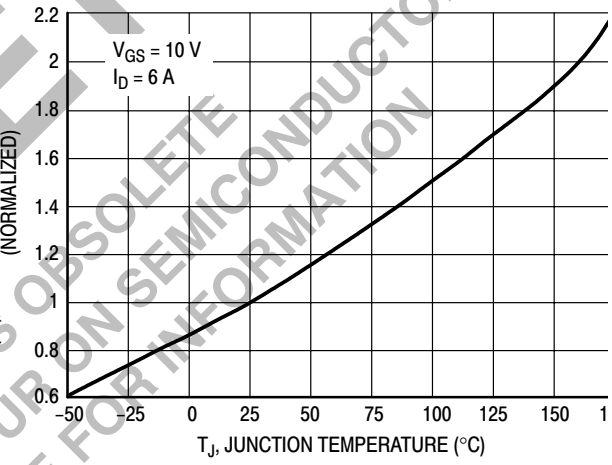
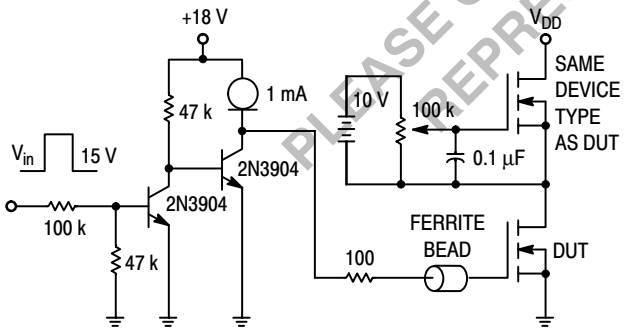


Figure 4. On−Resistance Variation with Temperature



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%.

Figure 5. Gate Charge Test Circuit

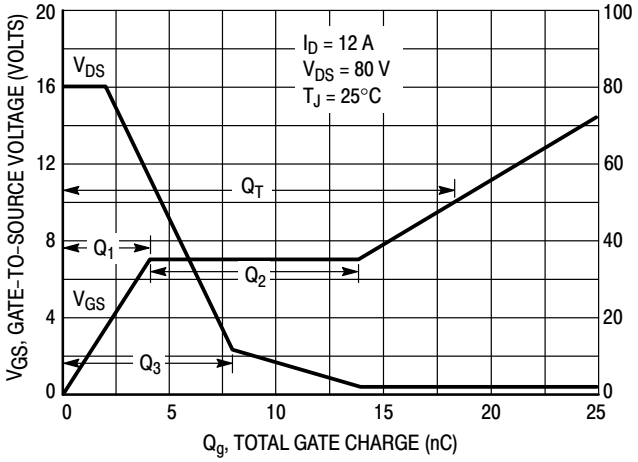


Figure 6. Gate−To−Source and Drain−To−Source Voltage versus Gate Charge

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance−General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 9 is applicable for both turn−on and turn−off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

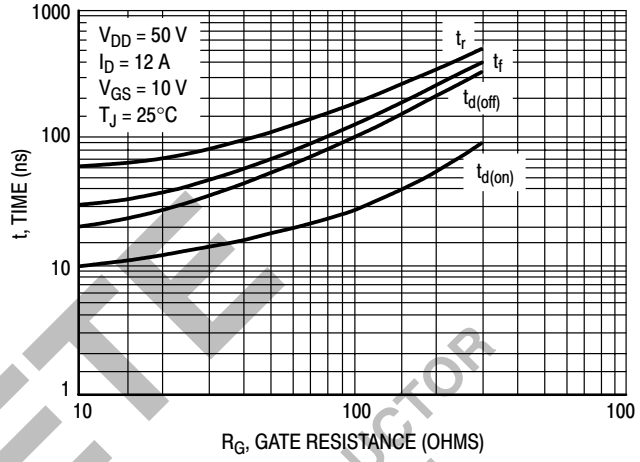


Figure 7. Resistive Switching Time versus Gate Resistance

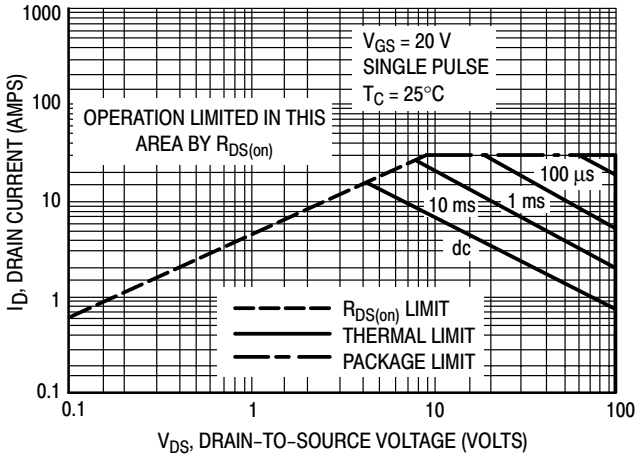


Figure 8. Maximum Rated Forward Biased Safe Operating Area

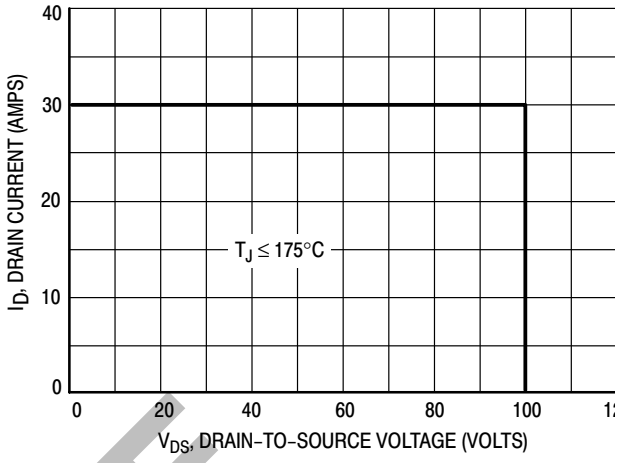


Figure 9. Maximum Rated Switching Safe Operating Area

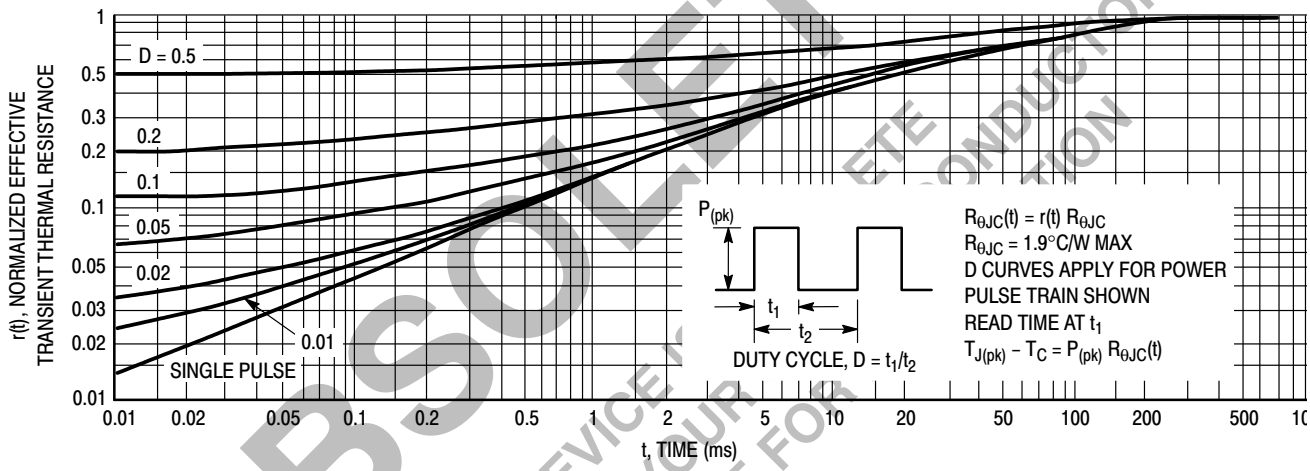


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain−to−source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums.

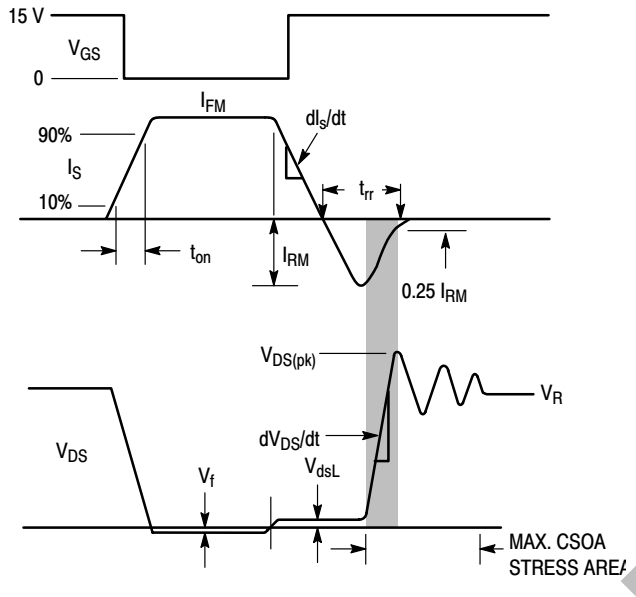


Figure 11. Commutating Waveforms

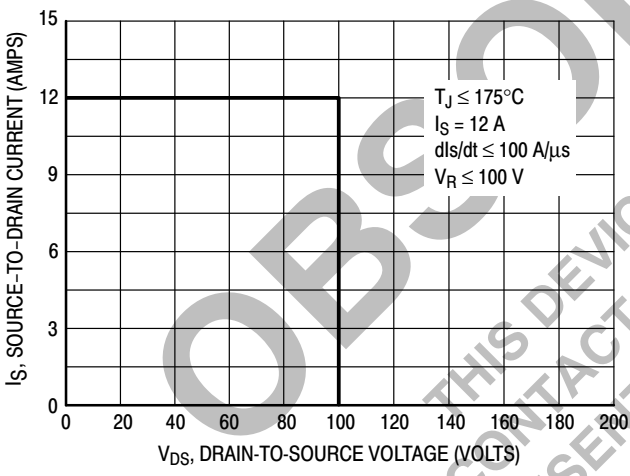


Figure 12. Commutating Safe Operating Area (CSOA)

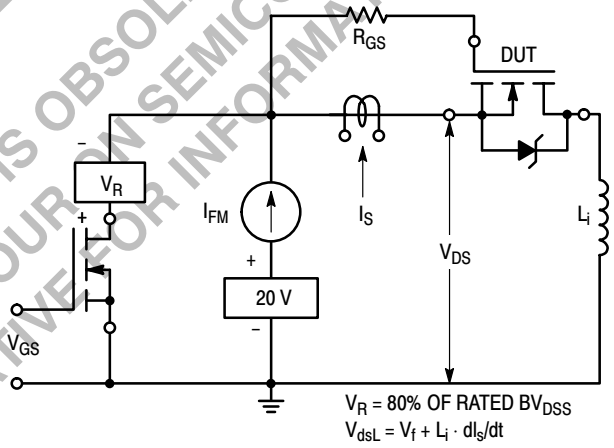


Figure 13. Commutating Safe Operating Area Test Circuit

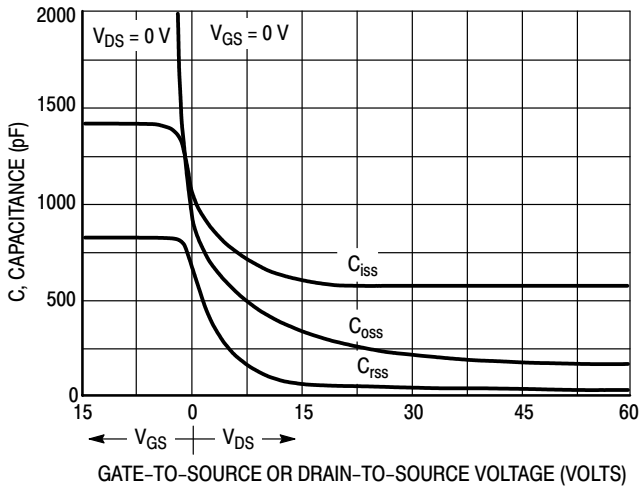


Figure 14. Capacitance Variation

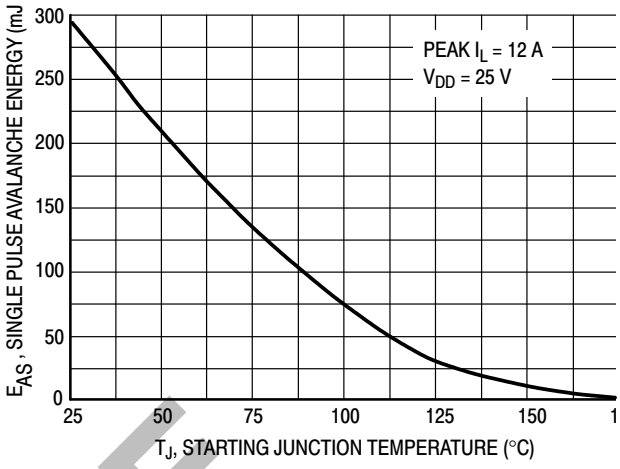


Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature

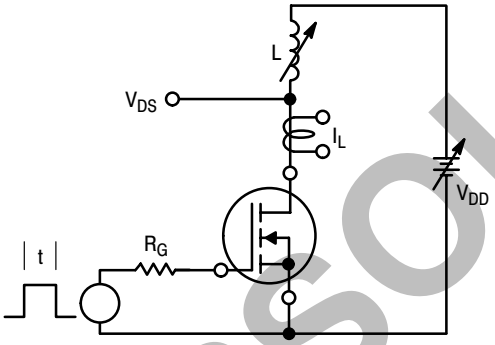


Figure 16. Unclamped Inductive Switching Test Circuit

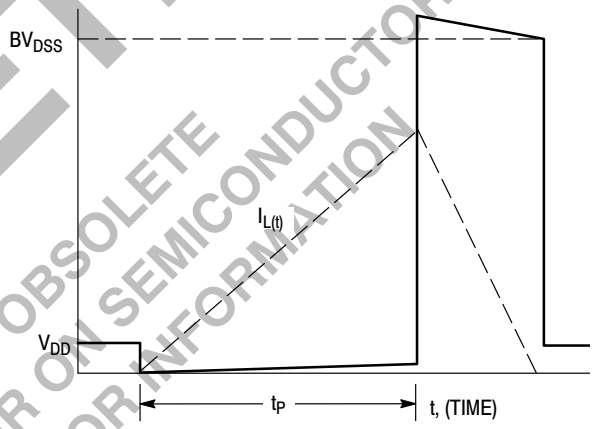
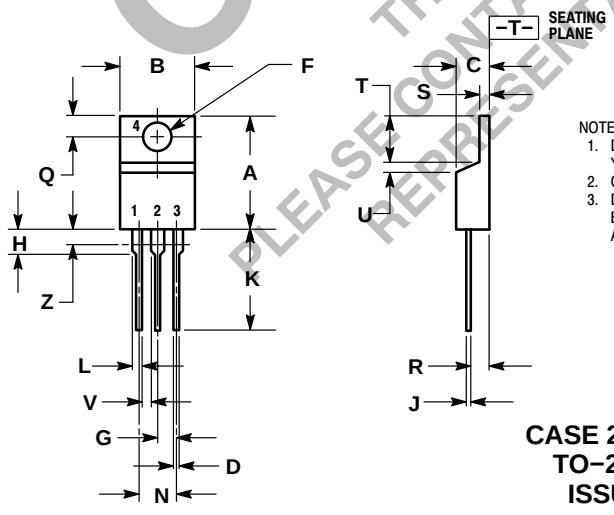


Figure 17. Unclamped Inductive Switching Waveforms

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

CASE 221A–06
TO–220AB
ISSUE Y

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